A General Mathematical Model for the Simulation of Common Faults in Three-phaseVoltage Source Inverters

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Abstract

In the last years the fault problem in power electronics has been more and more investigated both from theoretical and practical point of view. This paper analyzes the problem of faults modeling in a three phase voltage source inverter(VSI) and presents a model of a VSI able to simulate both unfaulty and faulty conditions when one or more devices go broken. In the past the fault problem was faced step by step considering the fault on each single device building a model for each case. The model hereafter presented solves this drawback through the introduction of the concept of the Healthy Device Binary Variable (HDBV) and the more general Healthy Leg Binary Variable (HLBV) showing also as through them it is possible to build a single model including all the running conditions (faulty and unfaulty) of a VSI. The presented model was then tested via numerical simulations by comparison of the results with those obtained with a circuit simulator and finally by comparison with experimental results on a set-up test bench realized to test the operating conditions of a three phase VSI.

Keywords

Numerical models; Faults; Fault-tolerance; PulseWidth Modulated Inverters

Nomenclature

j = {A, B, C} phase index;

$v_{jO(N)}$; ij phase voltages and currents on the AC side;

hj± upper(+)/lower(-) healthy device binary variables (HDBV);

hj healthy leg binary variables (HLBV);

Sj± upper(+)/lower(-) side transistor switching function for phase j;

Sj± upper(+)/lower(-) side transistor generalized switching function for phase j;

Dj± upper(+)/lower(-) side diode switching function for phase j;

U_{DC} whole inverter capacitor bank voltage;

U_1, U_2 partial capacitor bank voltage;

i_0 DC side inverter input current;

R_0,L_0 DC side wires parasitic circuit parameters;

C value of the single DC - Link capacitor;

R,L load circuit parameter ;

I diagonal eye matrix;

$[...]^t$ transposition of a matrix (a vector);

$\mathbf{1} = [111]^t$ unitary three-dimensional vector;

$\mathbf{u}_{ref}$ vector of the reference voltage in PWM control;

$\mathbf{u}^*_{ref}$ vector of the reference voltage in PWM control after a fault;

$\mathbf{v_k}$ vector of the converter output voltages;

$\mathbf{h}$ vector of the healthy leg binary variables;

$\mathbf{i_k}$ vector of the load currents;

$\mathbf{S_k}$ vector of the switching functions $[S_A, S_B, S_C]^t$;

$\mathbf{v}_1 \times \mathbf{v}_2$ cross product between generic vectors $\mathbf{v}_1$ and $\mathbf{v}_2$;

$\otimes$ Logical AND operator;

$\oplus$ Logical OR operator;

$\overline{(\ldots)}$ Superscript line denoting the logical NOT operator.

Introduction

In the last years a massive usage of power converters can be noted in many different application. Electrical drives, static power compensators, FACTS devices, renewable energies have gained great advantages of the technological improvements achieved in power electronics, as for new devices, as for new circuits, control systems and protection strategies [6]. However, faults remains unavoidable in each case, being the main cause for power system interruptions, obviously not considering that for scheduled maintenance [14]. These interruptions are also a cause of power deteriorations, damages and economical losses in the managements of electrical energy. [6], [3].

The main part of the power converters faults still regards the single devices on which diagnosis and repairs are not easy, so a fault occurrence implies long time in which the power converter must remain out of service.This is particularly true for all that system that makes a massive use of integrated power electronics boards [5,8,12].

From another point of view, the studies on faults are to be considered still in full evolution even if a great amount of technical literature is actually available, but it is clear that some questions are still waiting for an answer and many issues are still under a careful consideration by the researchers.

The paper is summarized as follows: Section 3 states the most important aspects of the problem. Sections 4 and 5 present the general model after the introduction of a generalized switching function, including the consideration of the conduction state for free-wheeling diodes. Section 6 shows simulation results of the presented model considering two types of fault: the fault on a single controllable device and the fault of both the controllable device and the corresponding free-wheeling diode. Section 7 validates the model via a second simulation realized through a circuit simulator avoiding the risks to power apparatus and laboratory operators due to a strong and long stress caused by the fault conditions. Finally, Section 8 summarizes conclusions.

Problem Statement

A fault investigation always implies the consideration of the effect of the faults on power devices, on the passive components of the system and on the networks and apparatuses to which the power converter is connected.

The approach followed in the most part of the technical literature is to consider each fault as a separate case without a general vision even in the modeling problem. In other words, in the modeling sector, each fault is considered as a single possible event and a corresponding model has been presented. In this way the simulation of an incoming fault condition implies the usage of two different models at least, and the simulation results have to be finally merged to achieve the behavior of a power system including a fault in power electronics devices. This means often to stop the simulations made with the unfaulty model, to collect the final value of the state space using it as the initial state for the second model (at faulty condition) and to start the simulation again with it. This is clearly unsuitable for many computation issues and, above all, really time consuming.

Furthermore, simulations are really important to study the transient behavior of a power system under fault to determine what are the most critical and dangerous conditions that may also cause the fault propagation within the power converter devices and then to the external components of the power system. These system models are really large and the stepped setting of its internal state to merge the final results is a really time consuming task.

The study of transients is also important because on its

results, the best active and passive actions to protect the systems against the effects of the fault and its eventual propagation are chosen. For this reason, the concept of a general model able to run in different conditions without and external actions, is fundamental in research and in set-up tools for designers able to run in the least time possible without a lack of accuracy [9].

To determine such a model let consider that faults in

power electronics are essentially due to short circuits on silicon devices (generally causing the destruction of oneor more components) and open circuits faults due to control or drive failures, i.e. with a loss of the switching pulses for each interested device.

Short circuit faults are very fast and, in general, no software algorithm is able to detect them in the short time required to interrupt and insulate them from the rest of the system. For this reason they are generally managed directly with hardware additional device or circuits and interrupted with ultra fast fuses, taking care that these last ones should not introduce

additional inductances in the main circuit, so compromising the speed of their intervention [10].

Different considerations apply for open circuits faults, being them more easy to detect and face. However it must be also considered that a short circuit faults evolution converges always to an open circuits condition in a very small time. In this way their effect on transients are often negligible, while the open circuit condition is maintained, so affecting the transient behavior of the whole power system [10,5,8]. such these considerations, the reason for which only open circuits fault only and their effects are considered in the present paper are clear.

Whatever the fault nature can be, diagnosis systems are so really important in conjunction with all those strategies allowing a system to continue its operation with and acceptable degree of power quality saving and an acceptable degree of performance, without any additional risks as for the rest of the devices and apparatuses as for people. These systems with such an ability are usually called fault-tolerant. In particular, in the present paper, the main topic is linked to fault-tolerant converters.

The availability of mathematical model of fault-tolerant converter is the key point to better investigate their design and their strategy for fault sensing and protection allowing their fast improvement.

The model proposed by the Authors in this paper is not new (see e.g. [2]), but the related results were tested and verified for a long time, so, actually they can be considered as mature and fully validated for the definitive presentation.

In general, traditional converter models include only the faulty or the healthy mode, resulting then not able to predict transient phenomena caused by faults occurrence.

The model hereafter presented overcomes this drawback. It is formulated by introducing the concepts of “Healthy Device Binary Variables” (HDBV) and "Healthy Leg Binary Variables" (HLBV). Such variables allow the management of both unfaulted and faulted conditions regardless of what is the faulty phase.

In general, in the past, both the cases of converter fault

and reconfiguration were considered individually. Instead the model hereafter presented allows the simulation of a faulty or not Voltage Source Inverter (VSI) and, furthermore, considers also the reconfiguration for a fault tolerant operation and all its effects [2].

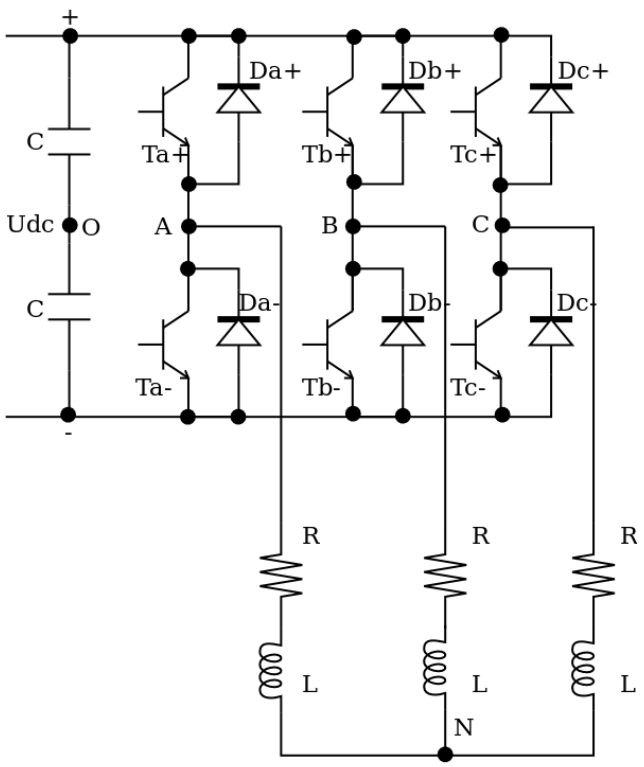

FIGURE 1 THE VSI TOPOLOGY

The General Vsi Modeling Via the Switching Function Theory

In the most part of technical literature power converters (and in particular the VSI of fig. 1) are sketched as a set of active components with instantaneous commutation for which it is possible to define some “Switching Functions” (SF). After the SF definition, the remaining part of the converter and of the power system is considered with the set of equations for passive components, coming out from the application of the Kirchhoff principles. The classical converter SFs for upper devices are defined as follows [11],[9],[6];

$$\begin{aligned} S_{j+} &= 1 \text{ if a driving pulse is given} \\ S_{j+} &= 0 \quad \text{otherwise} \quad \text{with j} = A,B,C \end{aligned} \tag{1}$$

Complementary SFs are defined for the lower device

Sj_;

In the case of VSIs every SF does not implies an effective conduction of the corresponding component because of the free-wheeling diodes, whose state

depend on the current sign. For this reason a second more general SF is introduced. Consider the upper active device of the j-th leg. An upper diode conducts the negative current only if the lower controllable device is switched off. In this way, the SF for the upper diode is:

$$D_{j+} = \overline{S_{j-}} \otimes (i_j < 0) \quad (2)$$

In a similar manner, for the lower diode, the corresponding SF is:

$$D_{j-} = \overline{S_{j+}} \otimes (i_j > 0) \quad (3)$$

In this way by summarizing the current signs, two generalized SFs may be defined:

$$\begin{aligned} \hat{S}_{j+} &= \left[S_{j+} \otimes (i_j > 0)\right] \oplus \left[\overline{S_{j-}} \otimes (i_j < 0)\right] \\ \hat{S}_{j} &= \left[S_{j-} \otimes (i_j < 0)\right] \oplus \left[\overline{S_{j+}} \otimes (i_j > 0)\right] \end{aligned} \quad (4)$$

In (4) the term at the left of the OR operator regards controllable devices conduction while the right one regards the diode conduction. This is natural by considering that an equivalent bidirectional switch includes the conducting transistor or diode.

The output voltage with respect to the O point, as sketched in fig. 1, is written as:

$$v_{jO} = \left(\hat{S}_{j+} - \hat{S}_{j-}\right)\frac{u_{DC}}{2}; \quad (5)$$

If the load impedances are balanced, the phase to neutral (N point) voltages have the well known expressions:

$$v_{jN} = v_{j0} - \frac{\sum_{k=j} v_{k0}}{3}; \quad (6)$$

The load currents can be found as the solutions of the integral equations:

$$i_j = \frac{1}{L}\int (v_{jN} - Ri_j)d\tau \quad (7)$$

To achieve a complete inverter model, DC Link circuit equations are considered. In particular the expression of the DC Link voltage is:

$$u_{DC} = \frac{1}{C}\int \left(i_0 - \sum_{k=j} i_k \hat{S}_k \right) d\tau \quad (8)$$

and i_0 is given by:

$$i_0 = \frac{1}{C}\int (u - u_{DC} - Ri_0)d\tau \quad (9)$$

Equations (4) - (9) summarize the model of a VSI in the healthy mode. All current and voltage equations were put in the integral form being it the easiest way for the simulation of a dynamical system.

The next subsection introduces the modified model for the faulty mode.

The Modeling of Inverter under Faulty Conditions

Starting from the previous equations it is possible to investigate the open circuits faults achieving useful considerations for a unique general modeling. It is clear that in the faults management the concept of generalized SF is very powerful and important.

Let us suppose that a controllable upper device go to a drive failure condition. In this case the SF S_{j+} is always null. A positive current cannot be conducted by any device in the faulted phase. On the contrary, the negative current may circulate in the upper diode and in the lower controlled device. Starting from diode conduction, if the lower device is switched off a natural commutation appears, then the diode current turns to zero while the transistor current rise up. In this case the generalized SFs for both upper and lower devices become [17,16,13,4]:

$$\begin{aligned} \hat{S}_{j+} &= \overline{S_{j-}} \otimes (i_j < 0) \\ \hat{S}_{j-} &= S_{j-} \otimes (i_j < 0) \end{aligned} \quad (10)$$

In particular S_{j+} includes only the upper diode conduction; S_{j-} includes the transistor conduction after it has been turned on.

Similar considerations apply when the faulted device is the lower. In this case the general switching functions become:

$$\begin{aligned} \hat{S}_{j+} &= S_{j+} \otimes (i_j < 0) \\ \hat{S}_{j-} &= \overline{S_{j+}} \otimes (i_j < 0) \end{aligned} \quad (11)$$

For the general case we define the *healthy device binary variable* (HDBV) as follows:

$h_{j\pm} = 1$ if the upper (+)/lower (-) device is healthy

$h_{j\pm} = 0$ otherwise （12）

The introduction of the HDBV makes the definition of the generalized (i.e. in faulty and unfaulty mode) switching function very simple. In fact, it results:

$$\begin{aligned}\hat{S}_{j+} &= \left[h_{j+}S_{j+} \otimes \left(i_j > 0\right)\right] \oplus \left[h_{j-}\overline{S_{j-}} \otimes \left(i_j < 0\right)\right] \\ \hat{S}_{j-} &= \left[h_{j-}S_{j-} \otimes \left(i_j < 0\right)\right] \oplus \left[h_{j+}\overline{S_{j+}} \otimes \left(i_j > 0\right)\right]\end{aligned} \quad (13)$$

In a general simulation scheme it is sufficient to multiply each $S_{j\pm}$ by the corresponding variable $h_{j\pm}$.

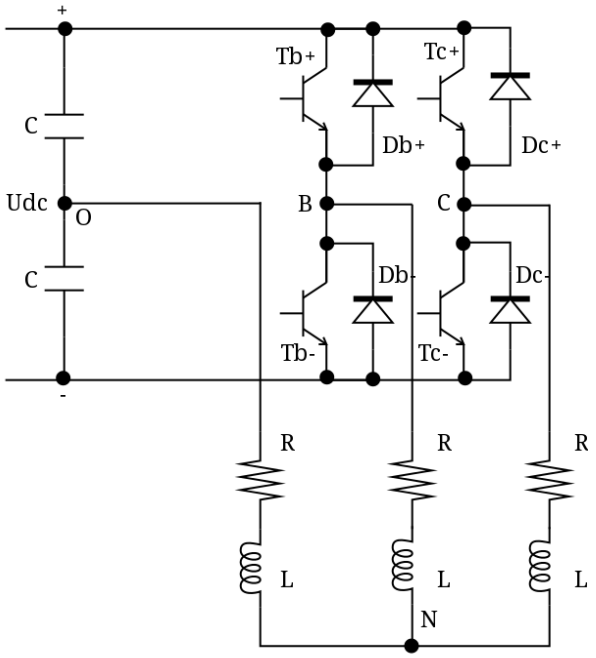

FIGURE 2: THE RECONFIGURED VSI FOR FAULT TOLERANT OPERATION

The same principle applies when both the transistor and the diode are broken, but the first expression of (10) now contains two non compatible conditions. However, the signal of (10) may be used to reset the integrator of (7). In this way, when the lower power device is switched off the load current is forced to zero. This is a dangerous condition for a power converter because of the over-voltages on power devices. In general the snubber circuit are able to absorb the surges coming out from the transient overlapping phenomena [10], [18], [15], [8], [13].

Finally, let us consider the case in which a whole inverter leg is loosen.This case does not introduce any difference with respect to the previously considered ones, because the approach with HDBVs allows an easy and affordable modeling in inverter reconfigured for fault tolerant mode. With this purpose, the healthy leg binary variables (HLBV) are then introduced as follows [2]:

$$h_j = h_{j+} \otimes h_{j-} \quad (14)$$

i.e. a leg is considered as faulted if the upper or the lower device is broken.

In reconfiguration, after fault diagnosis, the faulted leg is disabled and the load terminal of the faulted phase is connected to the middle point of the DC Link allowing the current circulation by means of bidirectional switches realized with triacs (see fig. 2).

These variables resume the fault cases, but they also are

suitable for the modeling of the fault-tolerant operation

after the converter reconfiguration (see fig. 2).

The presented model allows to consider the following

events chain:

1. Fault occurrence;
2. Its effect on the active and passive components of the converter;
3. Its effect on the external system (if its model is effectively available);
4. Effect on the reconfiguration of the converter to gain the fault-tolerant mode;
5. Transients behavior and effect on the converter itself and on the external power system.

In previous papers of the Authors [9], [6], [4], [1], this reconfiguration has been extensively discussed and the general model of the reconfigured inverter has been also presented.

In particular even the fault-tolerant system equations may be expressed as functions of the HLBV as follows:

$$\begin{aligned}U_1 &= \frac{1}{C}\int\left(i_0 - \hat{\mathbf{S}}_k^t \mathbf{H}_k^t \mathbf{i}_k\right)d\tau \\ U_2 &= \frac{1}{C}\int\left(i_0 - \hat{\mathbf{S}}_k^t - \mathbf{1}^t\left(\mathbf{I} - \mathbf{H}_k\right)\mathbf{i}_k\right)d\tau\end{aligned} \quad (15)$$

for the partial DC Link voltages with:

$$\mathbf{H}_k = \begin{pmatrix} h_A & 0 & 0 \\ 0 & h_B & 0 \\ 0 & 0 & h_C \end{pmatrix} \quad (16)$$

and

$$v_{kN} = \mathbf{TH}_k \left(\mathbf{1} \frac{U_2}{U_{DC}} + \hat{\mathbf{S}}_k \right) U_{DC} \quad (17)$$

for the inverter output voltages with respect to the load neutral point, and where:

$$\mathbf{T} = \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \quad (18)$$

In the fault-tolerant mode, the inverter has only two reference voltage signals with a displacement angle of 60 degrees. By using the defined HLBVs it is possible to synthesize a general control for the fault-tolerant inverter, including both faulted and unfaulted conditions: The reference voltage is synthesized with the vector equation:

$$\mathbf{u}_n * \quad = \lambda \mathbf{u}_n + \sqrt{3} \left(\overline{\mathbf{h}} \times \mathbf{u}_n \right) e^{-j\frac{\pi}{2}} \quad (19)$$

where:

λ = hAhBhC = det(Hk), and $\overline{\mathbf{h}}$ is simply the vector NOT(h) un* is the new reference voltage system and un is the older one (before the fault and the reconfiguration). The exponential termcompensate the instantaneous $-\pi/2$ phase jump in the references after the reconfiguration.

The control algorithm can run also in unfaulted conditions [9], [10], [17]. In fact at a no fault operation it result clearly $\mathbf{u}_n^* = \mathbf{u}_n$.

It is also interesting to note that such a definition of the post fault reference voltages is also useful when the converter run under a closed loop control system. In fact as the reference voltage system under faulted condition is expressed as in (19) the fault become invisible to the control loop because this last one has always to synthesize a three-phase reference that will be modified by the faulttolerant algorithm only if necessary. From another point of view, a good set up of the control loop will achieve a fast system response reducing the entity of the transient phenomenon and its duration after the reconfiguration of the converter.

Simulation Results in The Matlabsimulink ® Programming Environment

For the modeling test the MATLAB-SIMULINK® programming environment, now recognized as a standard de facto, has been used in this paper. The particular matrix approach of the model is really suited to the implementation because MATLAB® itself is optimized to solve a wide variety of problem in matrix form. Furthermore this model formulation does not require any specific additional MATLAB® toolbox for its implementation and solution. The SIMULINK® block scheme is shown in fig. 3.

In the following simulation the following cases are considered:

1. Drive failure on a single device with current circulation on the free-wheeling diode corresponding to the interrupted device;
2. Simulation of a faults on both the controllable device and its free-wheeling diode;
3. Converter reconfiguration after a fault and faulttolerant mode.

The considered electrical quantities are voltages on

faulted and unfaulted phases and the three phase load

currents. In the simulation an IGBT VSI with a 300V DC Link voltage is considered.

Figure 4 shows the output voltage on the faulted phase of the load for a driver failure in an upper device, while fig. 5 shows the currents on the load after the same fault.

These simulations show the positive current interruption and the negative current which flows through the diode. During the current interruption, the average value of the phase voltage is zero (the instantaneous value is made up of a series of voltage spikes only). The other currents on unfaulty phases become phase-opposite, as the applied voltages are an half of the line to line voltage with opposite signs.

Figure 6 shows, instead, the unfaulted phase voltage.

Figures 7 and 8 show the same results when the fault

regards both the device and the corresponding freewheeling diode.

The voltage is very similar to that of the previous analyzed case except for a higher number of spikes. Currents are, instead, quite different being composed of a series of negative pulse due to commutation of the lower transistor. The unfaulted phase voltage is very similar to the previous one and, for this reason, is not reported here.

The next simulation results report the effect of the

inverter reconfiguration and operation in fault tolerant mode. Figures 9 and 10 show the voltage in faulty and unfaulty phase while fig. 11 shows the current patterns before and after reconfiguration. The same fig.11 shows clearly the transient following the fault detection and reconfiguration of the converter.

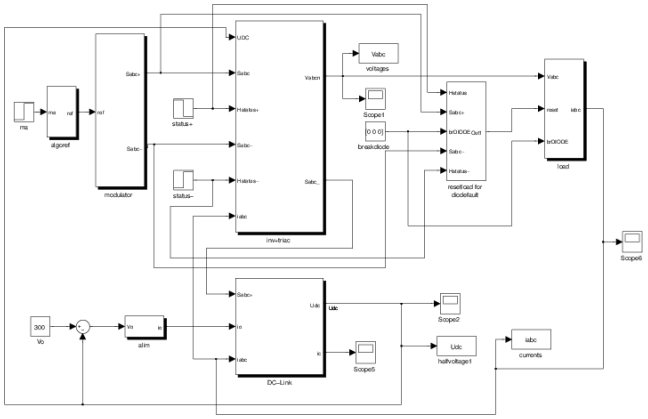

FIGURE 3 SIMLULINK® BLOCK DIAGRAM OF THE GENCONERAL VERTER MODEL

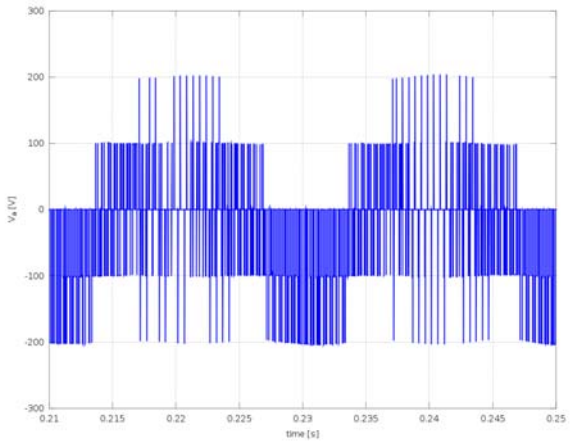

FIGURE 4 VOLTAGE ON LOAD FAULTED PHASE FOR UPPER DEVICE DRIVE FAILURE

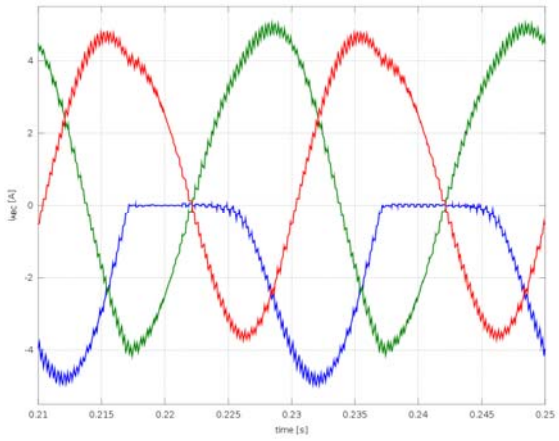

FIGURE 5 CURRENTS ON THE LOAD AFTER THE FAULT

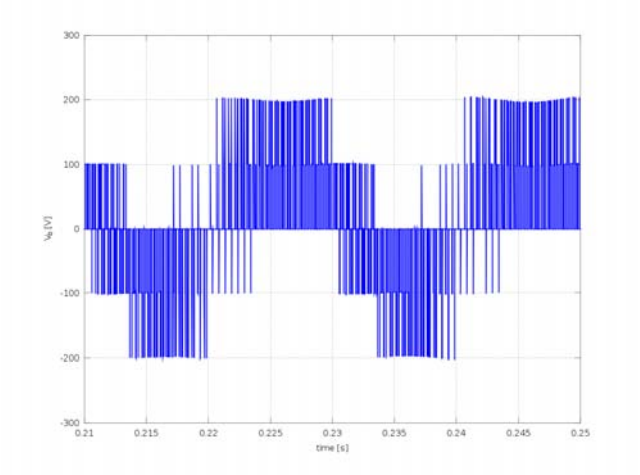

FIGURE 6 VOLTAGES ON AN UNFAULTY PHASE

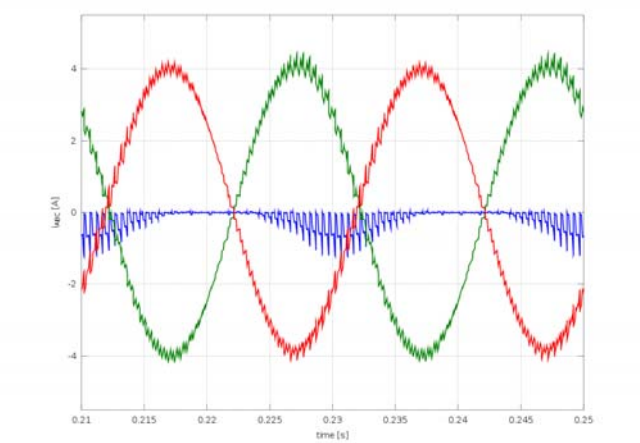

FIGURE 7 LOAD CURRENTS AFTER TRANSISTOR AND DIODE BREAKDOWN

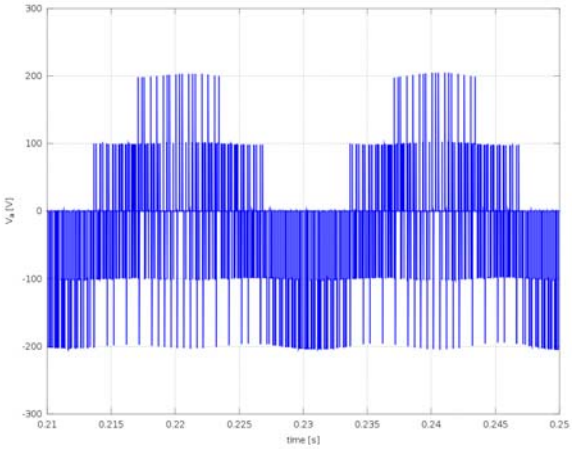

FIGURE 8 FAULTY PHASE VOLTAGE AFTER TRANSISTOR AND DIODE BREAKDOWN

Validation of the Model Via Further Numerical and Experimental Tests.

As it was said before, the final validation of the presented model is made through further numerical simulations and experimental results. The first were

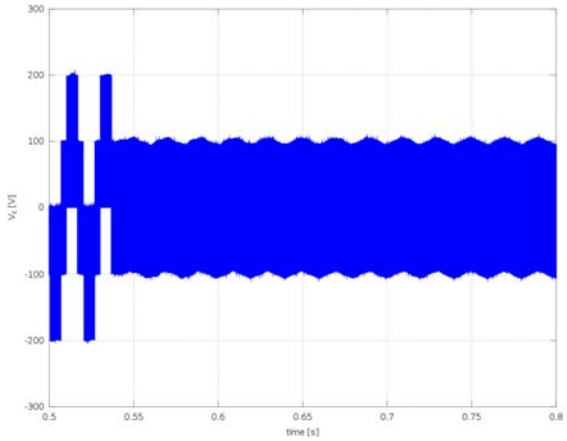

FIGURE 9: VOLTAGE AT FAULTY PHASE BEFORE AND AFTER FAULT OCCURRENCE

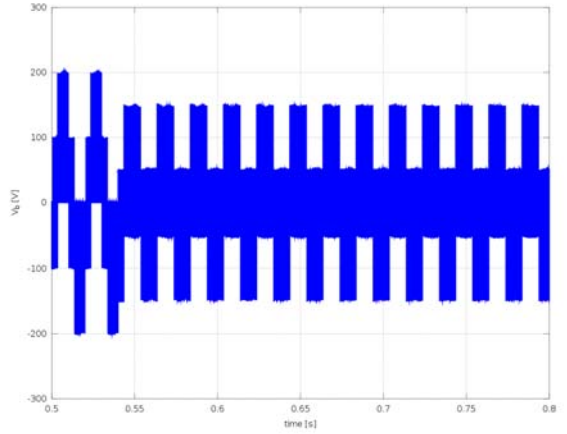

FIGURE 10VOLTAGE AT UNFAULTY PHASE BEFORE AND AFTER THE FAULT OCCURRENCE

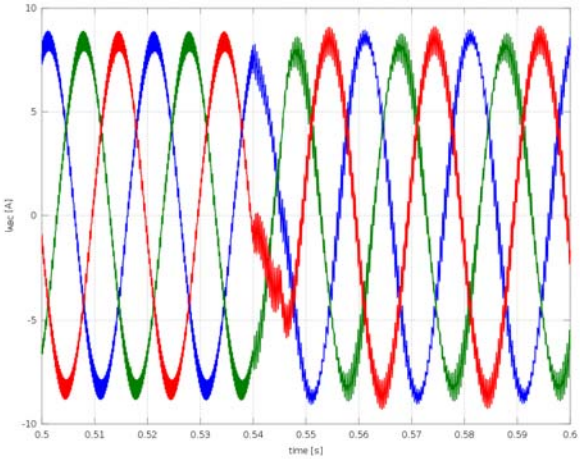

FIGURE 11CURRENTS PATTERNS BEFORE AND AFTER FAULT OCCURRENCE AND RECONFIGURATION

made to verify the model without risks for devices and people due to continuous operation under fault. The latter were made after the implementation of the fault tolerant mode in which the fault is insulated and avoided with no risks. For the second simulation set the SYM POWER SYSTEM®, a MATLAB-SIMULINK® toolbox operating like many other similar circuit simulators (see also, PSPICE®, EMTP®, CIRCUIT® MAKER® etc.) directly by the circuit layout, without writing any system equation. The presented model will be so validated by comparison of the results considering the SYM POWER SYSTEM® affordability recognized in the scientific area for its results accuracy.

Figures 12 and 13 show simulation results made with SYM POWER SYSTEM®.

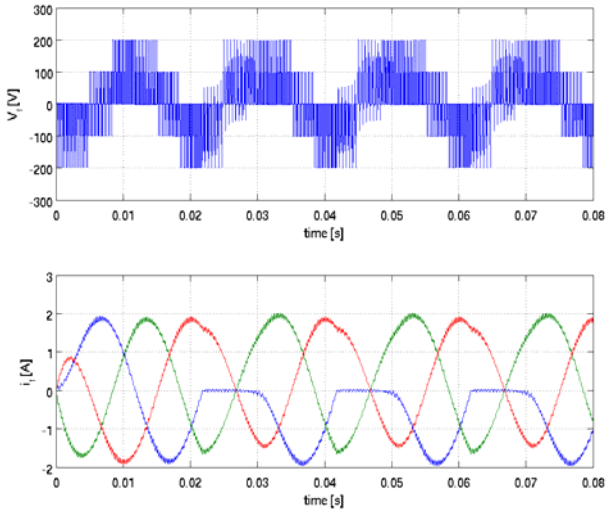

FIGURE 12 SIMULATION MADE WITH THE SYM POWER SYSTEMS TOOL (UNFAULTY PHASE VOLTAGE AND CURRENT)

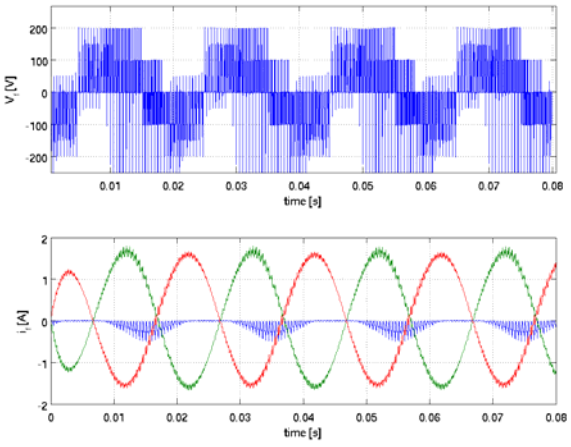

FIGURE 13 SECOND SIMULATION WITH THE SYM POWER SYSTEMS TOOL (FAULTY PHASE VOLTAGE AND CURRENT)

With complete evidence from the figures, the results are in excellent accordance with those obtained via the SIMULINK® package, but the Simulink simulation time amount is about 0.25 times that of SYM POWER SYSTEMS®.

Experimental results were, instead, made available in

the case of the fault tolerant converter operation, which can be considered as a safer one for a normal laboratory test.

For the experimental test, a customary benchmark based on an INFRANOR power converter and a dSPACE control board has been built and set up. The system load is a three phase induction motor.

For the experimental test, a customary benchmark based on an INFRANOR power converter and a dSPACE control board has been built and set up. The system load is a three phase induction motor whose nameplates are summarized in Table 1.

TABLE 1 INDUCTION MOTOR OF THE TEST BENCH NAMEPLATES

Power	5.5kW
Speed	2850 r.p.m
Torque	18.3Nm
Frequeny	50-60Hz
Voltage	400V
Currenct	13A

A digital oscilloscope with two differential probes (up to a 25-MHz bandwidth) and 3% accuracy have been used to register voltage and currents waveforms. Measurements data were stored in the same computer hosting the dSPACE board and finally plotted with the help of the "Octave" free software.

The fault emulation has been realized via solid state relays and connectors driven from the dSPACE board and its software interface. In this way it was possible to test the behavior of the fault-tolerant converter without a real disruption of the power devices.

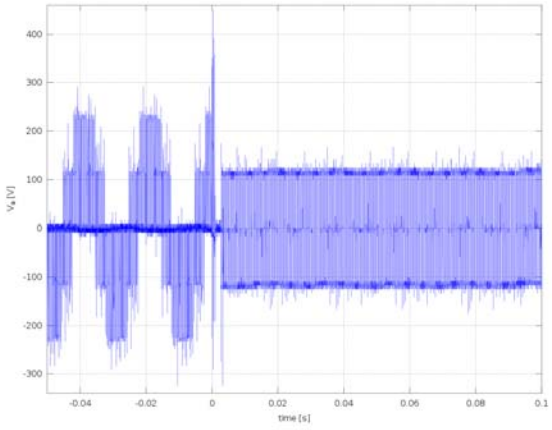

FIGURE 14 MEASUREMENT OF FAULTY PHASE VOLTAGE BEFORE AND AFTER THE FAULT

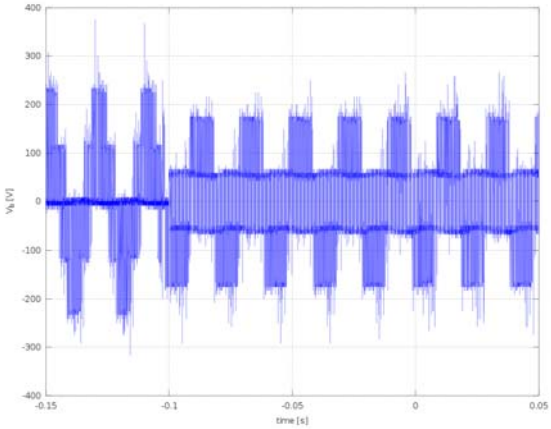

FIGURE 15 MEASUREMENT OF UNFAULTY PHASE VOLTAGE BEFORE AND AFTER THE FAULT

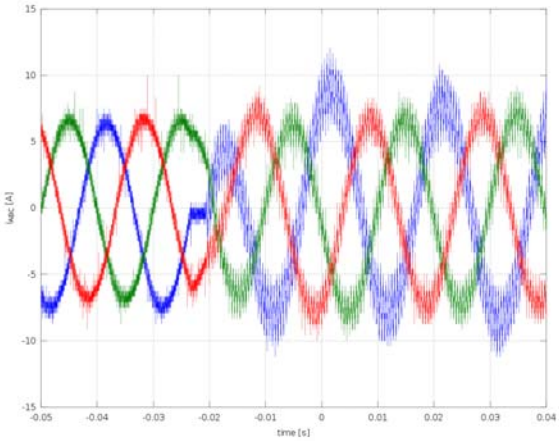

FIGURE 16 MEASUREMENTS OF PHASE CURRENTS BEFORE AND AFTER THE FAULT

Figures 14, 15 and 16 show respectively the measurements of voltage on faulty and unfaulty phases and the measurement of the currents, before and after fault and reconfiguration.

This final comparison validates the proposed general model of VSI in healthy and faulty mode.

Conclusions

The present paper has faced the system modeling problem for a faulted inverter limiting the attention to open circuits faults because they are very often a condition to which every fault evolves. In particular the problem was solved with the aim to find a unique and general model including the following situations:

- Healthy Inverter;
- fault on a single controllable device;
- fault on a single controllable device and its freewheeling diode;
- post fault inverter reconfiguration to run in fault

tolerant mode.

The considered cases gives an almost complete perspective on the different operating condition of an inverter allowing the study of the transients and of the steady state behavior of all the active and the passive converter components and eventually the behavior of the external power system achieving a wider vision.

With this purpose the concept of SF has been extended

and some suitable binary variables have been introduced (namely the HDBVs and the HLBVs) the to model the behavior of the single component and of the whole converter in the different situations including those of reconfigured converter.

It has been also demonstrated how the HLBVs are useful to control the converter in the fault-tolerant modes testing various control strategies.

The model verification has been made in the MATLABSIMULINK® programming environment, without the needs of any specific toolbox, by comparison of the numerical results with some others of the same system obtained with the SYM POWER SYSTEM toolbox (to be considered as acceptable for its recognized accuracy) with limitations to those cases for which the fault permanence is a risks for devices and people, and a further verification with experimental results in fault tolerant mode. The comparison of simulation and experimental results, with the clear good accordance between them, confirms definitely the validity of the proposed model.

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